CLAIMS

What is claimed is:

1. An input circuit for an RF power amplifier comprising:

an input network having a transformer with a primary side and a secondary side, wherein

an RF input signal is coupled to the primary side;

a limiting amplifier having an input coupled to the secondary side of the transformer and

an output for providing an input to the RF power amplifier; and

a DC feedback loop coupled to the limiting amplifier.

2. The input circuit of claim 1, wherein the limiting amplifier is comprised of a plurality of inverters connected in series between the limiting amplifier input and the limiting amplifier output.

3. The input circuit of claim 2, further comprising an amplifying stage coupled between the input of the limiting amplifier and the transformer.

4. The input circuit of claim 1, further comprising an amplifying stage coupled between the input of the limiting amplifier and the transformer.

5. The input circuit of claim 4, wherein the amplifying stage is comprised of a common-source amplifier.

6. The input circuit of claim 4, wherein the amplifying stage is comprised of a common-gate amplifier having one or more switching devices.

7. The input circuit of claim 6, wherein a bias is provided to a gate terminal of each of the one ore more switching devices.

8. The input circuit of claim 7, wherein the bias is a DC bias.

9. The input circuit of claim 6, wherein a dynamic bias is provided to the gates of the switching devices.

10. The input circuit of claim 6, wherein the RF input signal is coupled to both the source and gate of one or more of the switching devices of the amplifier stage.

11. The input circuit of claim 6, wherein the common gate amplifier has two switching devices, and wherein the RF input signal is coupled to both the source and the gate of each of the two switching devices.

12. The input circuit of claim 1, wherein the RF power amplifier is formed on a semiconductor substrate, and wherein the input circuit is formed on the same semiconductor substrate.

13. The input circuit of claim 12, wherein the semiconductor is a complementary metal oxide semi-conductor (CMOS) semiconductor.

14. A predriver circuit for an RF power amplifier comprising:

an input circuit coupled to an RF input signal; and

a plurality of inverters coupled in series between the input circuit and an input of the RF power amplifier.

15. The predriver circuit of claim 14, further comprising an amplifying stage coupled between the plurality of inverters and the input circuit.

16. The predriver circuit of claim 14, wherein the amplifying stage is comprised of a common-source amplifier.

17. The predriver circuit of claim 14, wherein the amplifying stage is comprised of a common-gate amplifier having one or more switching devices.

18. The predriver circuit of claim 17, wherein a bias is provided to the gates of the switching devices.

19. The predriver circuit of claim 18, wherein the bias is derived from the output of the RF power amplifier.

20. The predriver circuit of claim 18, wherein the bias is derived fromboth the input and the output of the RF power amplifier.

21. The predriver circuit of claim 18, wherein the bias is set to cause the DC bias levels of the input and the output of the RF power amplifier to be approximately equal.

22. The predriver circuit of claim 14, wherein the inverters are CMOS inverters.

23. A method of controlling a power amplifier having a predriver circuit comprising:
sensing the input and output DC levels of the power amplifier;
comparing the sensed DC levels;
creating a feedback signal based on the difference between the sensed DC levels; and
adjusting the DC bias levels in the predriver so that the input and output DC levels of the power amplifier are maintained in a predetermined relationship.

24. The method of claim 23, wherein the feedback signal is a negative feedback signal.

25. The method of claim 23, wherein the DC bias levels in the predriver are adjusted so that the input and output DC levels of the inverting power amplifier are approximately equal.

26. The method of claim 23, wherein the power amplifier is an inverting power amplifier.

27. An amplifier comprising:

a transformer having a primary side and a secondary side, the secondary side having first and second terminals, wherein the primary side is adapted to receive an input signal;

a first switching device having first and second nodes, the first node coupled to the first terminal of the secondary side of the transformer;

a second switching device having third and fourth nodes, the third node coupled to the second terminal of the secondary side of the transformer;

a first capacitance coupled between the second node of the first switching device and the third node of the second switching device; and

a second capacitance coupled between the first node of the first switching device and the fourth node of the second switching device.

28. The amplifier of claim 27, wherein the first and third nodes are source nodes of the switching devices.

29. The amplifier of claim 28, wherein the second and fourth nodes are gate nodes of the switching devices.

30. The amplifier of claim 27, wherein the input signal is an RF input signal.

31. The amplifier of claim 27, further comprising a current path for allowing DC current to flow through the first and second switching devices.

32. The amplifier of claim 31, wherein the current path is provided by coupling a voltage reference node through a center tap formed in the transformer.

33. The amplifier of claim 31, wherein the current path is provided by one or more inductors coupled between the first and third nodes of the switching devices and a voltage reference node.